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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,472	08/26/2003	Lawrence M. Burns	1875.3770001	2309

26111 7590 12/12/2006

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,472	BURNS ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/02/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,11,12,14 and 15* is/are rejected.

7)☒ Claim(s) *3, 6-10, 13 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 2, 2006 have been fully considered but they are not persuasive.

The applicants' argue: *"Nowhere does Adams teach or suggest that the output of the test circuit is used to correct for parameters in the operational portion of the chip."*

In response to the above argument, the examiner disagrees with the applicants. In col. 4, line 62-col. 5, line 27, in col. 6, line 34-col. 7, line 25 and in col. 9, lines 16-34, discuss comparing the on-chip signal to the set signal from an external source to determine if the signal are the same when the semiconductor device is being tested. Therefore, the examiner believes that Adams suggests what is being claimed.

The applicants' further argue: *"In addition, neither the on-chip signal nor the test signal received by the test circuit of Adams represents a process dependent integrated circuit parameter."*

In response to the above argument, the examiner disagrees with the applicants. First, the examiner will like tot thank the applicants for explaining what is meant by "process dependent integrated circuit parameter". However, the applicants must keep in mind MPEP 2111 states a claim must be interpreted in light of the specification without reading limitations into the claim. With using the word "parameter", it is not specific of the meaning of process dependent integrated circuit and therefore the examiner is giving the limitation the broadest reasonable interpretation. Regarding claim 11, the applicants must keep in mind also MPEP 2114 states that while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguish from the prior art in terms of structure rather than function alone. Therefore, the examiner believes that Adams suggests what is being claimed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-5, 11-12 and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Adams et al (6163862).

Regarding claims 1 and 11, Adams et al disclose [see Figs. 1 and 3] a system for monitoring an integrated circuit chip (semiconductor device 10), comprising: means for receiving (test circuit 30 and sense amplifier 18) at least one digitized sense signal (on-chip signal 26) from the integrated circuit chip (10), whereby the at least one digitized sense signal (26) represents a corresponding process-dependent parameter within the integrated circuit chip (10); and means for determining (test circuit 30) an analog value for the at least one process-dependent circuit parameters from the corresponding at least one digitized signal (26); wherein the process-dependent parameter is measured within a process monitor portion (sense amplifier 18) of the integrated circuit (10) and the at least one determined analog value is utilized to correct for the process-dependent parameter in an operational portion (memory cells 12) of the integrated circuit (10).

Regarding claims 2 and 12, Adams et al disclose the means for receiving (30) and the means for determining (30) are positioned external of the integrated circuit chip (10).

Regarding claims 4 and 14, Adams et al disclose the means for determining (30) comprises means for calculating the at least one value from the at least one digitized signal (26).

Regarding claims 5 and 15, Adams et al disclose the at least one digitized sense signal (26) represents a gate-to-source threshold voltage of a transistor [shown in Fig. 1A] fabricated on the integrated circuit chip (10).

Conclusion

4. Claims 3, 6-10, 13 and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 3 and 13, the reason for allowance of the claims is a system and method for monitoring an IC chip comprises, in combination with other limitations, means for determining comprises means for retrieving the at least one value from a look-up table using the at least on digitized signal.

Regarding claims 6-10 and 16-20, the reason for allowance of the claims is a system and method for monitoring an IC chip comprises, in combination with other limitations, the at least one digitized sense signal includes a plurality of digitized sense signals that represent a plurality of the following: a transconductance parameter of a transistor fabricated on the integrated circuit chip; a sheet resistance of a resistor fabricated on the integrated circuit chip; a temperature of the integrated circuit chip; and a power supply voltage on the integrated circuit chip.

Base on the arguments, the following is being applied.

6. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
December 8, 2006